

# **A 5T SRAM with Improved Read Stability and Variation Tolerance over 6T**

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A Thesis

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by

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August 2008

## **APPROVAL SHEET**

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Master of Science (Computer Engineering)

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## Abstract

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As technology scales according to Moore's law, the stability of the conventional Static Random Access Memory based on a 6-transistor bitcell (6T SRAM) suffers drastically, especially during the Read operation. In addition, there is a perennial demand for better performance, in terms of memory access time. Finally, shrinking device dimensions leads to increasing inter-die and intra-die variation, which makes memory design even more challenging.

The goal of this thesis is to achieve better stability measured in terms of Static Noise Margin (SNM) during read, better performance in terms of memory access time during read and higher tolerance to variation than the conventional 6T SRAM, without sacrificing area. We present a 5-transistor (5T) SRAM that achieves these objectives by exploiting the inherent asymmetry of the bitcell. It does so by appropriately sizing the cross-coupled inverter pair in the bitcell. Alternatively, a 5T bitcell that is constructed by simply removing one access transistor from a 6T bitcell has similar metrics as the 6T, but saves on area. Moreover, the asymmetric 5T SRAM scales well with technology and offers increasing improvement in the aforementioned metrics relative to the 6T SRAM. All this comes at the cost of a lower write margin when compared to a 6T SRAM.

A test chip with a 4 kb 5T SRAM was fabricated in a commercial 90 nm technology and was found to read and write correctly. Another test chip with a 48 kb 5T SRAM and a 16 kb 6T SRAM in a 45 nm technology has been sent for fabrication.

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## List of Symbols

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$C_{ox}$	Capacitance per unit area of gate oxide .....	29
$CR$	Cell Ratio .....	50
$k$	Boltzmann Constant .....	29
$k_n^*$	Process Transconductance Parameter .....	53
$L$	Transistor Channel Length .....	20
$PR$	Pull-up Ratio .....	52
$q$	Charge on an electron in Coulombs .....	29
$T$	Temperature in Kelvin .....	29
$V_{DS}$	Transistor Drain to Source voltage .....	29
$V_{DSAT}$	Transistor velocity saturation voltage .....	54
$V_{GS}$	Transistor Gate to Source voltage .....	29
$V_{SB}$	Transistor Source to Bulk voltage .....	54
$V_T$	Transistor threshold voltage .....	29
$V_{T0}$	Transistor threshold voltage without body effect .....	54
$W$	Transistor Channel Width .....	20
$\gamma$	Body effect coefficient .....	54
$\Delta V$	Voltage ripple at memory cell storage node containing 0, when writing 1 .....	50
$\mu_0$	Mobility of a carrier at 0 Kelvin .....	29
$\mu_n$	Mobility of electrons .....	51
$\mu_p$	Mobility of holes .....	51
$\eta$	Drain Induced Barrier Lowering (DIBL) coefficient .....	29

$\phi_F$	Fermi potential .....	54
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# Chapter 1

## Introduction

---

### 1.1 Introduction

Static Random Access Memories or SRAMs as they are popularly known are a major component of any state of the art digital circuit. The data storage units or bitcells in conventional SRAMs are composed of 6 transistors (6T). This chapter discusses the motivation for this thesis, which presents an SRAM containing bitcells that are composed of 5 transistors (5T). It also provides an outline and potential contributions of this thesis. Finally, it presents a glossary of the terminology used in this thesis.

### 1.2 Motivation

As technology scales according to Moore's law [1], shrinking transistor dimensions and supply voltages, designing memories becomes increasingly challenging. Firstly, the stability and reliability of the bitcell both when it is holding data or being read reduces. Static Noise Margin (SNM) is the most frequently used metric for bitcell stability. Reduced SNM during a read operation limits scaling of the traditional 6T bitcell to lower supply voltage ( $V_{DD}$ ) and to new technologies. Numerous read assist methods are available in the SRAM peripheral circuits to improve noise margins, e.g. [2] [3] [4]. These methods lower the wordline voltage or raise the cell  $V_{DD}$  to increase read margins. However, these methods are not scalable and may not work if the peripheral circuits change.

Alternatively, 8 transistor (8T) cells that buffer the storage node in the bitcell have been proposed to replace the 6T cell, e.g. [5] [6], although they require additional transistors that increase area. Secondly, the demands for higher performance and speed, in terms of memory access time during read and write operations are ever increasing. In addition, the burgeoning embedded and mobile electronics industry necessitates even smaller chip areas. Finally, as device dimensions shrink, the effect of inter-die and intra-die variations increases. In particular, shrinking widths and lengths of transistors increases the variability (standard deviation) of the distribution of threshold voltage ( $V_T$ ) of the transistors in the SRAM. Consequently, the distributions of various stability and performance metrics are spread wider. This requires digital circuit designers to look farther out into the tails of the distributions for the worst cases and design for these worst cases to meet yield requirements. Ultimately, this leads to conservative and pessimistic designs, which consume more area and power than necessary, for a majority of the chips produced. Thus, in addition to improving the mean Read Static Noise margin and read access time, it is important to reduce variability in these metrics as well.

We propose a 5T bitcell that uses sizing asymmetry to improve the Read SNM and reduce read access time without increasing bitcell area. In addition it reduces variability in the read access time. Previous works have proposed this same 5T schematic [7] [8] [9]. The next chapter discusses relevant work in greater detail. We propose a new way of using the 5T cell to improve Read SNM without decreasing speed or increasing area.

### 1.3 Potential Contributions

This thesis can make the following contributions.

- A methodology to increase Read stability in terms of Read Static Noise Margin.
- A methodology to increase performance in terms of access time during read.
- A methodology to reduce SRAM area.
- A methodology to reduce the impact of global and local variations on SRAM design.

## 1.4 Outline of Thesis

- **Chapter 1 - Introduction:** Introduction, motivation and overview of the thesis. Also includes brief description of terminology used in the thesis.
- **Chapter 2 - Related Work:** This chapter describes relevant earlier work.
- **Chapter 3 - 5T basics:** This chapter presents the schematic of the 5T, the basic idea behind the sizing strategy of the 5T bitcell. It also describes the read and write operations for the 5T bitcell.
- **Chapter 4 - Comparison of 5T vs 6T:** This chapter compares 5T noise margins, drive current, read delay and other important metrics with those of a 6T.
- **Chapter 5 - Solving the Write Problem:** This chapter describes the write problem with the single-ended 5T bitcell. A methodology to work around this problem is presented.
- **Chapter 6 - Test Chip Implementation:** This chapter describes the fabricated 90nm test chip and measurement results.
- **Chapter 7 - Conclusions:** Conclusions, contributions of this work and future work are described in this chapter.
- **Bibliography** - A list of references used in this thesis.

## 1.5 Terminology

The following is an alphabetical listing of terms and abbreviations used in the thesis:

**5T:** A bitcell composed of 5 transistors.

**6T:** A bitcell composed of 6 transistors.

**bitcell(cell):** Basic unit of an SRAM that stores one bit of data. Essentially composed of a cross-coupled inverter pair and zero or more access ports or transistors.

**BL:** Bitline, a wire that connects the bitcell, possibly through an access transistor, to the sense amplifiers and the Bitline drivers which supply the data during a write.

**BLB:** Bitline-bar, a complementary Bitline, present in a conventional 6T bitcell.

**CMOS:** Complementary MOS, circuits that contain both NMOS and PMOS devices.

**HSNM:** Hold Static Noise Margin, a measure of cell stability during hold, measured using static/dc sweeps.

**Leakage:** In this thesis, refers to sub-threshold leakage, which is the current flowing between the drain and source of a transistor when it is in the off-state, that is the gate of the transistor is below the threshold voltage.

**MC Simulation:** Monte Carlo simulation, the technique of simulating a circuit over a wide range of randomly chosen values for device parameters [10].

**MOS(FET):** Metal Oxide Semiconductor Field-Effect Transistor, a transistor that uses a metal-oxide as an insulator between a polysilicon gate and a semiconductor. An electric field can be used to create an inversion layer or channel between the source and drain terminals of the transistor.

**NMOS:** A MOSFET that utilizes an n-type inversion layer for conducting current.

**PMOS:** A MOSFET that utilizes a p-type inversion layer for conducting current.

**RSNM:** Read Static Noise Margin, a measure of cell stability during read, measured using static/dc sweeps.

**Sense Amplifier:** An analog circuit that amplifies a differential voltage. It is used to speed up reading by sensing and amplify the differential between BL and BLB. It also helps in avoiding the energy overhead of fully discharging the bitlines which have large capacitances.

**SNM:** Static Noise Margin.



**SRAM:** Static Random Access Memory, which stores data statically using a cross-coupled inverter pair.

**Transistor:** Refers to a MOSFET in this thesis.

**trip point:** Refers to the input voltage of an inverter, for which the output voltage is the same as the input voltage.

**VDD:** Reference for the high potential power supply (1.0 V in this thesis).

**VSS:** Ground, reference for the low potential power supply (0 V).

**VT:** Threshold voltage, the voltage at which the channel in a transistor undergoes strong inversion and begins conducting.

**VTC:** Voltage transfer characteristic, a curve that plots the output voltage of a system versus its input voltage.

**WL:** Wordline, a wire that controls the gates of the access transistors of a bitcell.

**WNM:** Write Noise Margin, a measure of cell stability during write. Also, a measure of the ease with which the cell can be written.

**Yield:** The percentage or proportion of devices on the wafer that are found to perform properly.

**Read Upset:** Overwriting the data in a bitcell when reading it, due to insufficient Read SNM.

# Chapter 2

## Related Work

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### 2.1 Introduction

The idea of a 5T bitcell is not new and 5T bitcells with different capabilities and methods of operation have been proposed in the past. This chapter briefly describes some of the 5T bitcells that have been proposed earlier. We also look at how the 5T proposed in this thesis is different from the earlier ones. Appendix A describes the schematic and operation of the conventional 6T SRAM and familiarizes the readers with some of the terminology that is used in this chapter. Readers unfamiliar with SRAM terminology are encouraged to read it before proceeding with this chapter. The glossary presented in Chapter 1 is recommended as well.

### 2.2 Earlier designs of the 5T bitcell

This section discusses three 5T bitcells - [7] presents a 5T SRAM with an intermediate bitline precharge voltage, [8] presents a 5T SRAM which employs a floating ground technique to achieve single-ended write and finally, [9] presents a completely different 5T bitcell, one that has no access transistors.

### 2.2.1 A 5T bitcell with mid-rail BL precharge

Carlson et al. [7] proposed a 5T SRAM which focuses primarily on saving area and reducing leakage power. They propose a different sizing strategy in order to solve the single-ended write problem, which is the challenge of writing the bitcell through a single access transistor. Chapter 5 describes this problem in depth. Figure 2.1 shows their proposed 5T bitcell in  $0.18\mu\text{m}$  technology. This sizing strategy reduces the trip point of the inverter M2-M4 and raises that of the inverter M1-M3. The access transistor is sized to be much stronger than the drive transistor, which enables a write “1” by simply driving BL high, as in a conventional 6T. The write “0” operation is also similar to the conventional 6T, namely, driving BL low and asserting the WL. However, this sizing strategy will certainly result in a read upset, which is the flipping of a cell’s contents when reading from it. In order to solve this problem, the authors propose to use a carefully selected intermediate precharge voltage (600 mV, for  $V_{DD} = 1.8\text{V}$ ) for the BL during read.

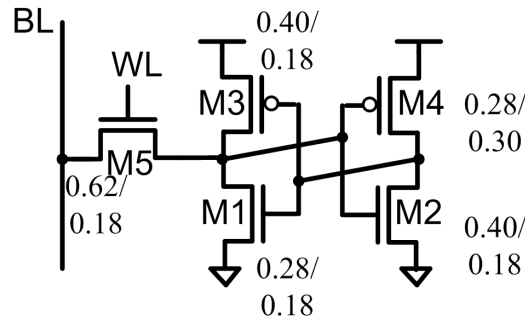


Figure 2.1: 5T bitcell with intermediate read BL precharge voltage [7]

Though the intermediate precharge voltage scheme enables a successful read and write in the typical case, the Read SNM suffers drastically. Even at the typical process corner, it is less than half the Read SNM of the 6T (Table 2.1). Moreover, the authors don’t explore the performance and stability of the cell in the presence of local variations. This is particularly important in current and future nanometer technologies due to the increasing impact of variation on circuit design. In fact, variation may make it impossible to select a precharge voltage that will work for a sufficient

number of bitcells, so as to satisfy the yield requirement.

Metrics	6T	5T
Read Time	499ps	421ps
Write Time	135ps	191ps
Read SNM	255mV	117mV
Leakage/cell	7.08nA	4.07nA
Cell Area (DRC)	7.99 $\mu m^2$	6.30 $\mu m^2$
Area (128Kb)	1.15 $mm^2$	0.88 $mm^2$

Table 2.1: 6T vs 5T at typical process corner, 110°C [7]

In this thesis however, the focus is on improving read stability and performance without affecting area. The 5T cell proposed in this thesis allows the designer to trade-off area savings with high statistical Read SNM in presence of variations, lower read access time and lower variability in the read access time. Monte Carlo simulations are used to verify the efficacy of the proposed design methodology in the presence of local variations.

### 2.2.2 A 5T bitcell with floating virtual ground

Tran presents a 5T bitcell in [8] which performs a single-ended write by floating the source of the drive NFET connected to the access transistor (Figure 2.2). We employ a method very similar to the one presented in this work. However, we go one step further and take advantage of the asymmetric 5T bitcell to improve other metrics such as read access time and read SNM.

The read operation for this 5T is the same as for the conventional 6T, since the SRC node in Figure 2.2 is grounded during a read operation. During a write operation, the signal WEX turns off the transistor  $M_{N5}$  and floats the source of  $M_{N2}$  to weaken the positive feedback in the cell. Now, a “1” can be written to the cell by driving BL high, provided the trip point of the inverter  $M_{P2} - M_{N3}$  is below  $V_{DD} - V_T$ . In order to retain the data written, the SRC node is restored to ground before the end of the the WL pulse. To achieve a significant write margin and prevent flipping the data in unaccessed cells due to the floating SRC node, the capacitance of the SRC node must be sufficiently high. For this, a large number of bitcells are required per bitline. This increases the delay of the SRAM. In the 5T SRAM presented in this thesis, a write method similar to the one in this work is

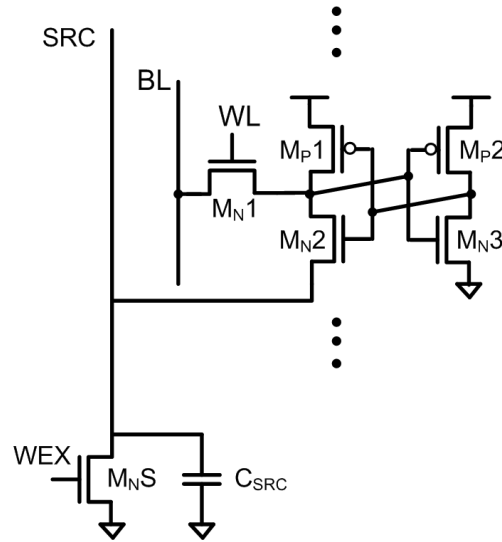


Figure 2.2: 5T bitcell with floating SRC node [8]

used, but it does not compromise the delay of the SRAM. Chapter 5 describes the write technique used in detail.

### 2.2.3 A portless 5T bitcell

The 5T SRAM presented in [9] is different from the ones presented previously in this chapter and the one proposed in this thesis in that it does not have an access transistor (port). That is, it is portless. The schematic of the cell is shown in Figure 2.3

The PFETs of the cross-coupled inverters are directly connected to the bit-lines and there is an additional transistor M5 coupling the inverters. The cell holds data in the cross-coupled inverters, with M5 off and no write signals applied to the column NFETs. The bitlines are charged to  $V_{DD}$  by the PFETs at the top of the columns.

During a read operation, only the access (AXS) signal of the selected cell is asserted to turn on M5 for that cell. M5 is weakened considerably by making it several times longer than the minimum length to preserve data during read. M5 creates a current path from the bitline to ground through the cell. The added current drawn from the PFETs at the top of the cell column creates a voltage differential on the BL pair that is sensed by a conventional sense amplifier.

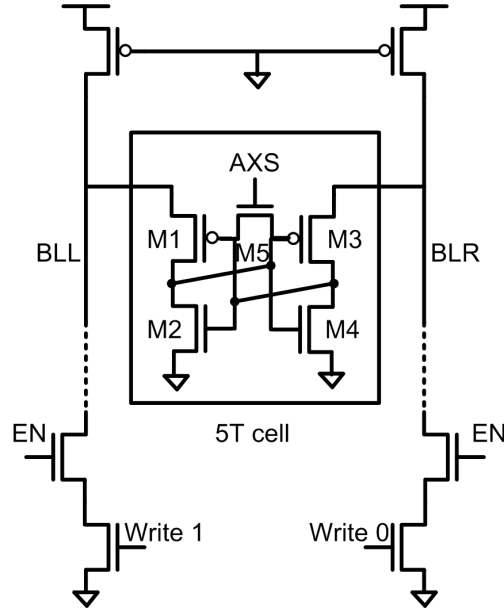


Figure 2.3: Portless 5T bitcell [9]

For writing the cell, the AXS signal is first asserted and the Write 1 or Write 0 signal is activated to pull one of the bitlines to around  $2/3V_{DD}$ . This reduces the current flowing through the cell and consequently, the voltage drop across M5. Thus, the cell NFET attached to the zero-node will turn on and the contents of the cell will flip to reflect the bitline data.

The portless 5T cell allows the designer to trade-off area with performance, stability and leakage power by changing the length of M5. Table 2.2 compares the portless cell to two conventional 6T designs in  $0.18\ \mu\text{m}$  CMOS at  $110^\circ\text{C}$ . The four portless 5T cells are matched to  $6T_b$  with respect to one of area,  $I_{Cell}$ ,  $SNM_{Read}$  and  $I_{Leak}$ .

Portless 5T cell matched by:						
Metric	$6T_a$	$6T_b$	Area	$I_{Cell}$	$SNM_{Read}$	$I_{Leak}$
Area ( $\mu\text{m}^2$ )	8.99	<b>8.64</b>	<b>8.77</b>	13.26	8.77	25.38
$I_{Cell}$ ( $\mu\text{A}$ )	152	<b>83</b>	59	<b>82</b>	46	87
Read SNM (mV)	252	<b>210</b>	303	596	<b>216</b>	550
$I_{Leak}$ (nA)	2.0	<b>1.8</b>	1.1	1.2	1.5	<b>1.9</b>

Table 2.2: 6T vs portless 5T [9]

Table 2.2 presents various metrics for two 6T cells and 4 portless 5T cells. Each of the portless 5T cells is matched to  $6T_b$  in terms of one of the four metrics — Area,  $I_{cell}$ , Read SNM and  $I_{leak}$ . The parameter by which the portless 5T is matched to the 6T is represented in bold. We see that in order to achieve similar  $I_{Cell}$  and consequently similar performance as the 6T, we need to compromise on area. The 5T cell with a similar drive current as the 6T has a 53% larger area. Conversely, a portless 5T that has roughly the same area as the conventional 6T suffers in terms of performance, though the Read SNM is improved. The portless 5T has 29% lower  $I_{Cell}$  than the reference 6T and thus a higher read access time, although this is compensated by nearly 3x increase in Read SNM and half the leakage.

As we will see in Chapter 4, the 5T cell presented in this thesis not only improves the mean statistical  $I_{Cell}$  in presence of variations, but also reduces the variability ( $\sigma$ ) in the  $I_{Cell}$  and consequently in the read access time. Unlike the portless 5T, this comes at no area penalty.

# Chapter 3

## 5T Basics

---

### 3.1 Introduction

This chapter gives a brief overview of the proposed 5T bitcell. We look at the structure of the 5T cell and briefly explore the read and write operations for the 5T. Next, we examine the basic idea behind the 5T and the methodology used to achieve considerable improvement in RSNM, when compared to the conventional 6T. Finally, we look at some layout options for the 5T bitcell and discover how it can either lead to area savings or improvement in stability and performance metrics.

### 3.2 Proposed 5T bitcell

#### 3.2.1 Schematic

A conventional 6T bitcell is shown in Figure 3.1. The proposed 5T cell is a conventional symmetric 6T bitcell with one access FET removed, as shown in Figure 3.2. We propose to access this 5T cell through the single access transistor in a fashion very similar to the normal 6T cell. Appendix A describes the conventional 6T bitcell in detail.

#### 3.2.2 The Read Operation

The read operation in a 5T bitcell is similar to a 6T bitcell. BL is precharged to  $V_{DD}$ . It is then allowed to float, and the WL is asserted. Depending on the data stored in the cell, the BL either



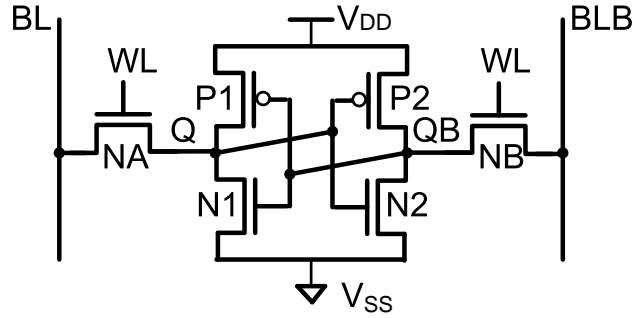


Figure 3.1: 6T bitcell schematic

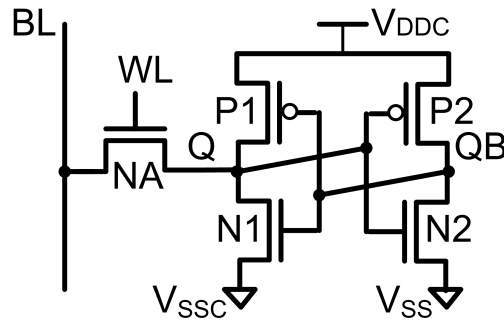


Figure 3.2: Proposed 5T bitcell schematic

starts discharging or remains at the precharged voltage, not taking into account leakage from the bitline into unaccessed cells storing “0”, through their turned-off access FETS. The drop in bitline voltage or otherwise then needs to be sensed or translated to a full swing “0” or “1”, in order to complete the read operation.

### 3.2.2.1 Reading a “0”

Figure 3.3 shows the equivalent circuit for a read “0” operation. Transistors N1 and P2 are on and their gates are at  $V_{DD}$  and ground respectively at the onset of the read operation. WL is initially off and the BL is precharged to  $V_{DD}$ . The capacitance of the BL is many orders of magnitude larger

than that of the cell, and is represented by  $C_{BL}$ . Then the BL is allowed to float and the WL is turned on. The potential difference between the precharged bitline and the node Q causes current  $I_{drive}$  to flow from the BL to  $V_{SSC}$ . The drive NFET, N1 and the access NFET, NA are sized to ensure that the voltage of node Q does not rise above the trip point of the inverter P2-N2 and thus flip the cell, causing a read upset. In other words, N1 is made stronger than NA. The drop in the BL voltage is then translated to a “0” by the read peripheral circuitry.

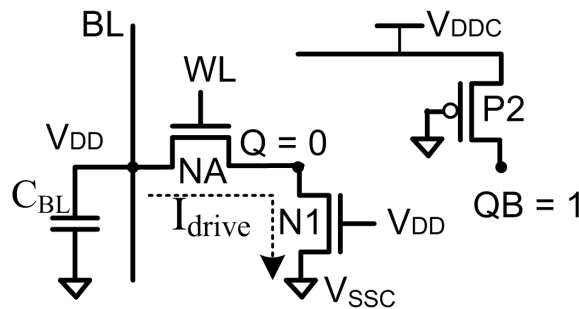


Figure 3.3: Simplified model of 5T cell at the onset of a read “0”

### 3.2.2.2 Reading a “1”

Figure 3.4 shows the equivalent circuit for a read “1” operation. At the onset of the read operation, transistors N2 and P1 are on and their gates are at  $V_{DD}$  and ground respectively. The BL is at its precharge value of  $V_{DD}$ . When the BL is released and WL driven high, the access transistor NA turns on. As the node Q is at “1”, there is no current flowing from the BL to ground since there is no potential difference across the access transistor. The BL voltage is then translated into a “1” by the read peripherals.

In the ideal scenario, BL remains at its precharged value. However, leakage into the bitline from the unaccessed cells storing a “0”, through their access transistors, causes the BL voltage to droop. The read peripherals must take into account this scenario and ensure that a “1” is not incorrectly read as a “0”. The effect of bitline leakage is further discussed in section 3.2.2.4.

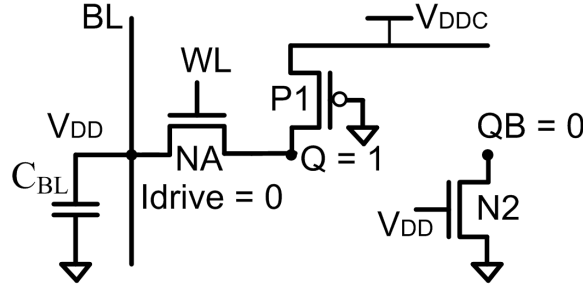


Figure 3.4: Simplified model of 5T cell at the onset of a read “1”

### 3.2.2.3 Completing the Read Operation

Sensing the read value is a challenge since the 5T is single ended. Consequently, differential sensing as for a 6T bitcell, cannot be directly used. However, we can convert the single-ended sensing problem to a differential sensing one. One idea would be to use a sample and hold scheme. In this scheme, the value of the BL before the WL is turned on, is sampled and used as a reference in a differential sense amplifier. Alternatively, a voltage reference can be generated on-chip to be used in the differential sense amplifier. However, creating a good reference source is not easy, since the voltage levels tend to vary from die to die or even over a single die. The reference source must therefore track those variations. Finally, there are several single-ended sensing schemes, such as [11], which can be used for a 5T SRAM.

Since the test chip was fabricated to test functionality only, it implements a full swing read using a dynamic inverter (Figure 3.5). Moreover, if short bitlines are used, with only a few bitcells per bitline, the performance overhead of using a full swing read is not too high. This was the case for the fabricated 5T SRAM in 90 nm technology.

The dynamic inverter in Figure 3.5 works as follows. Before the Read cycle begins, the dynamic inverter output (OUTB) is precharged by setting PDCH. If the bitcell stores “0”, upon activation of the WL, BL begins discharging. When it drops below  $V_{DD} - V_T$ , the load transistor PU turns on. OUTB goes high and OUT goes low. If the bitcell stores “1”, the BL stays at  $V_{DD}$  (neglecting

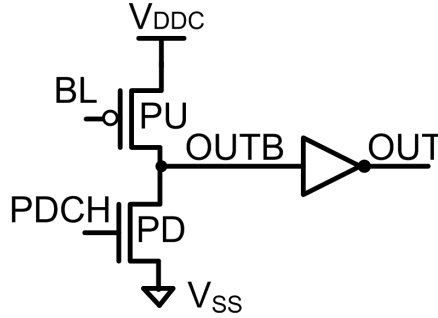


Figure 3.5: Dynamic inverter used for full-swing read

leakage). OUTB stays at the precharged value of 0 and OUT stays at 1.

The advantage of using a dynamic inverter over a static CMOS inverter to perform a full swing read is that it is much faster than the static inverter. The precharge of the dynamic inverter output ensures that reading a “1” is pretty fast. In addition, we don’t have to worry about factors such as sense amp offset voltage, making design easier and more robust. However, the sense amp is inherently faster as it works on small signal voltages and doesn’t wait for the bitline to discharge completely. Also, using a dynamic inverter can lead to erroneous reads due to bitline leakage and variation, as explained in the next subsection.

#### 3.2.2.4 Effect of Bitline Leakage and Variation

In general, when reading a “1”, the BL doesn’t stay at its precharged value of  $V_{DD}$ , but droops due to leakage into the unaccessed bitcells through their switched off access NFETs (Figure 3.6). In the worst case, all the unaccessed bitcells in the column store a “0”, which leads to a large amount of leakage from the BL into the bicell. This can cause the BL to droop below  $V_{DD} - V_T$  of the dynamic inverter’s PFET, leading to an erroneous read. For instance, if the  $V_T$  of the dynamic inverter’s PFET in a particular column is 0.4V,  $V_{DD} - V_T$  is 0.6V. If the bitline leakage from the unaccessed cells causes BL to droop below 0.6V, the dynamic inverter’s PFET turns on. As a result, OUTB goes high and OUT goes low, thus erroneously reading a “0”.

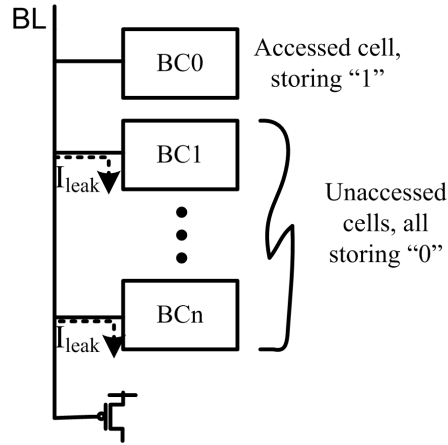
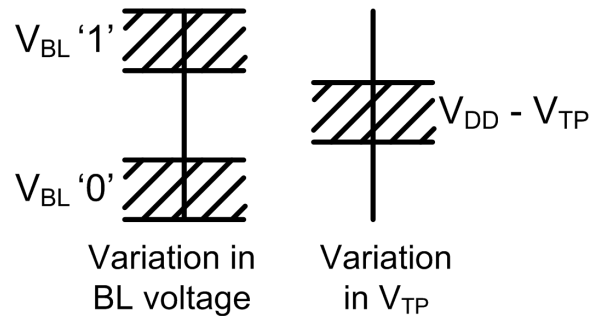


Figure 3.6: Worst case Bitline Leakage when reading a "1"

This problem worsens in the presence of variations in BL leakage and in the threshold voltage of the dynamic inverter's PFET. Figure 3.7 shows the ideal scenario for the BL and  $V_T$  variations to not affect the read. As shown, ideally the variation in  $V_{DD} - V_{TP}$  lies in between the possible variation of the BL voltage when either a "1" or "0" is being read. If the variation of the BL voltage overlaps with the variation of  $V_{DD} - V_T$ , the need to design for the worst case will lead to increasing device sizes to reduce variation. For example,  $V_T$  variation can be reduced by widening up the PU device in the dynamic inverter. This reduces the probability of overlap between the two variations. However, this increases area and power dissipation.

Figure 3.7: BL voltage and  $V_T$  variations: ideal scenario

### 3.2.3 Write Operation

#### 3.2.3.1 Writing a “0”

A '0' is written to the 5T bitcell in the same way as in a 6T. The BL is driven low and the WL is asserted. Figure 3.8 shows the equivalent circuit during a write “0” to the bitcell. We assume that the gates of transistors P1 and N2 stay at ground and  $V_{DDC}$  respectively, as long as the switching has not commenced. Though this condition is violated when the cell starts flipping, it is good enough for a rough analysis.

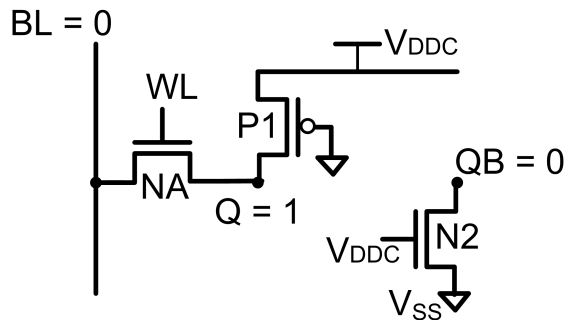


Figure 3.8: Simplified model of 5T cell at the onset of a write “0”

When the wordline is raised NA is turned on and current is drawn from node Q to BL. At the same time, however, P1 is still turned on and, as soon as the potential at the node Q starts to decrease, current will flow from  $V_{DDC}$  to the node. In this case NA has to be stronger than P1 to ensure that node Q flips. The transistor P1 is a PMOS transistor and inherently weaker than the NMOS transistor NA (the mobility is lower in PMOS than in NMOS). Therefore, making both of them minimum size according to the process design rules, or of equal size will ensure that NA is stronger and that writing is possible. When node Q has been pulled low enough, the transistor P1 will no longer be turned on and the node QB will also flip, leaving the cell in a new stable state.

### 3.2.3.2 Writing a “1”

However, writing a “1” is not straightforward. The sizing of N1 to avoid read upsets and the inherent inability of an NMOS transistor to pass a high signal makes this a challenge. For a 6T bitcell (Appendix A), this is overcome by writing a “0” to node QB through the complementary bitline, BLB. Obviously, this solution does not work for a 5T cell due to the absence of a complementary bitline. One idea would be to use circuit-level write-assist techniques, such as those presented in [2], [3] and [12]. Chapter 5 discusses this problem in detail and presents a methodology to write a “1” to the 5T bitcell.

## 3.3 Sizing strategy

Figure 3.9 shows the VTC “butterfly” curve of the symmetric 6T bitcell during a read operation. The voltage divider effect created by the “on” access transistors and the NMOS drive transistors squashes the lobes of the butterfly curve, which is still symmetric. The RSNM is defined as the side of the smaller of the largest squares that can be embedded in either of the lobes of the butterfly curve [13].

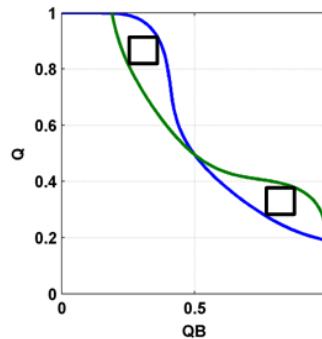
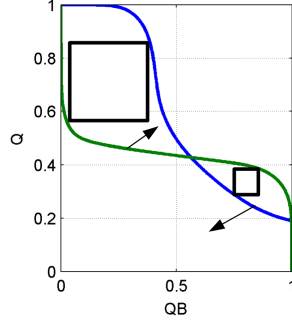


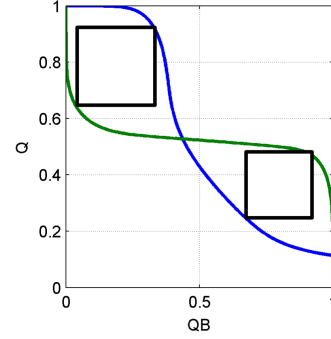
Figure 3.9: Read VTC curve for 6T bitcell

For the 5T bitcell derived from this symmetric 6T bitcell, only one of the lobes of the butterfly curve is squashed, as can be seen in Figure 3.10(a). This is due to the missing access FET. As a result, the largest square that can be embedded in one lobe of the curve is much larger than that can be embedded in the other. By sizing the cross-coupled inverters asymmetrically, we can increase

the RSNM considerably. Figure 3.10(b) shows the read VTC butterfly curve for the asymmetric 5T bitcell.



(a) Read VTC curve for unchanged 5T bitcell



(b) Read VTC curve for asymmetric 5T bitcell

Figure 3.10: Read VTC curves for 5T bitcells

We can introduce this asymmetry by strengthening (increasing the current conducting capacity of) N1 and P2 and/or by weakening P1 and N2. A transistor can be strengthened by widening it or reducing its channel length and weakened by narrowing it or increasing its channel length. As we can see from Appendix B, the current through a transistor is proportional to the  $W/L$  ratio of the transistor. Thus, introducing asymmetry by strengthening N1 has the additional advantage of increased current through the drive NFET during a read operation, and consequently lower read delay than the 6T.

Finally, increasing either the length or width of any device in the bitcell reduces standard deviation of the threshold voltage ( $\sigma_{VT}$ ), which is inversely proportional to  $\sqrt{\frac{1}{WL}}$ . This in turn, has the effect of reducing the spread of the RSNM, HSNM and Read delay distributions, thus increasing yield.

### 3.4 Layout

The missing access FET in the 5T creates a “notch”, which gives us the flexibility to either exploit this space to save area relative to the 6T, or increase the sizes of the other devices to make the areas equal and to improve upon certain metrics relative to the 6T. Figure 3.11 shows the layout of two



abutted bitcells. The dotted line indicates the two individual cells. The individual transistors of the bitcell are labeled.

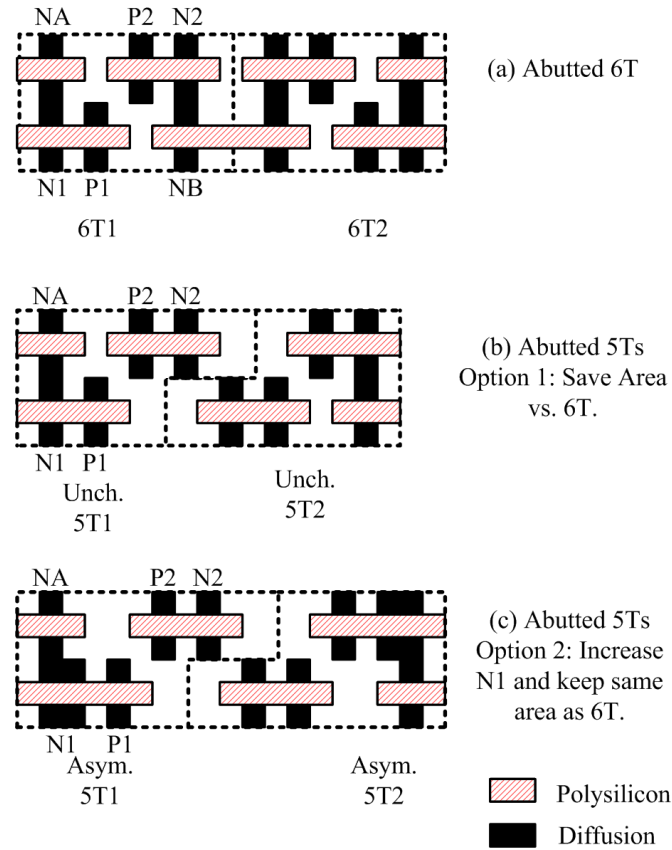


Figure 3.11: Example layout options for 5T bitcell

The layout in (a) shows two adjacent 6T bitcells. The layout of the 5T cell can be customized in two ways. Firstly, we can keep all transistor sizes the same, and thus save area, while maintaining or improving RSNM and read delay relative to the 6T bitcell (Option 1 in Figure 3.11). Alternatively, we can trade-off area with RSNM and/or drive current. For example, by widening N1 (e.g. Option 2 in Figure 3.11), we can increase RSNM and drive current. In addition, this increase in N1 width reduces the variability ( $\sigma$ ) of the distributions of these metrics in the presence of local variation.

In practice, CMOS logic design rules are not followed in commercial SRAM manufacture.

Instead, a different set of “pushed” rules is used for SRAM design, which allow even more compact design than can be achieved with standard logic Design Rule Checks (DRC). Since these rules are not available to us, we cannot accurately evaluate the area trade-offs. In general, the area trade-offs presented in this thesis can be assumed to be pessimistic. In other words, it is possible to achieve higher area savings than presented, if the sub-DRC SRAM rules are followed for layout.

# Chapter 4

## 5T vs 6T: A detailed comparison

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### 4.1 Introduction

This chapter presents the advantages of a 5T SRAM over the conventional 6T. In the analysis presented in this chapter, we compare a typical 6T bitcell with a 5T in terms of Area, Stability (Read and Hold), Performance (Read access time/Drive Current) and Leakage. The disadvantages are dealt with in the following chapter. Finally, we also discuss the impact of scaling on the 5T.

### 4.2 Area

This section compares the area of the 5T bitcell with different sizing strategies, with a reference 6T configuration.

#### 4.2.1 Bitcell Area

Table 4.1 shows the sizing (W/L ratios of each device) and bitcell area of the reference 6T bitcell and various 5T bitcells in 90 nm technology. The 6T bitcell chosen is sized so that the drive NFET is stronger than the access NFET, in order to prevent read upsets. 5T\_unchanged is the unchanged 5T derived from the reference 6T by dropping one access NFET. 5T\_sameArea is an asymmetric 5T which has a wider (stronger) N1 and a narrower (weaker) N2 , but the same total bitcell area as the reference 6T. However, it has a better RSNM and read delay, as we will see in the following

sections. 5T\_larger is an asymmetric 5T with a wider N1, a narrower N2 *and* a wider P2. This has moderately larger area than the reference 6T, but has considerably higher RSNM and read delay than the reference 6T.

Bitcell	$\frac{W_{P1}}{L_{P1}}$	$\frac{W_{N1}}{L_{N1}}$	$\frac{W_{P2}}{L_{P2}}$	$\frac{W_{N2}}{L_{N2}}$	$\frac{W_{NA}}{L_{NA}}$	$\frac{W_{NB}}{L_{NB}}$	Area ( $\mu m^2$ )
6T_ref	0.2/0.1	0.2725/0.1	0.2/0.1	0.2725/0.1	0.2/0.1	0.2/0.1	1.94
5T_sameArea	0.2/0.1	0.4/0.1	0.2/0.1	0.2/0.1	0.2/0.1	-	1.94
5T_unchanged	0.2/0.1	0.2725/0.1	0.2/0.1	0.2725/0.1	0.2/0.1	-	1.89
5T_larger	0.2/0.1	0.5/0.1	0.5/0.1	0.2/0.1	0.2/0.1	-	2.26

Table 4.1: Sizing and Area

We can see how the 5T gives the designer the flexibility to optimize area according to his requirements. If area is the primary concern, 5T\_unchanged can be used. If the requirement is to improve upon the stability and performance without sacrificing area over the 6T, 5T\_sameArea can be used. Finally, if the designer is willing to throw in a little extra area (16% in 5T\_larger), enormous improvement in stability and performance metrics can be achieved. This is explored in the following sections.

As mentioned earlier, it should be noted that the above area estimations are from a DRC compliant layout. If special SRAM DRC rules are followed, higher area gains can be achieved in the case of 5T\_sameArea and 5T\_unchanged, and the area penalty would be less than 16% for 5T\_larger.

#### 4.2.2 Chip Area

The area savings in terms of the bitcell cannot be directly translated to area savings in terms of the actual 5T SRAM chip area. This is because of the write “1” problem with the 5T (discussed in Chapter 5), which needs additional power supplies and logic. This leads to some area overhead. In the fabricated 90 nm chip, this overhead circuitry is about 20% of the bitcell array area. However, this includes a lot of testing logic. Moreover, the focus was on functionality and the layout was not optimized for area. In an actual 5T SRAM chip, the overhead would be much less than 20% if area optimization was carefully considered while laying out the chip. Since an area optimized 5T

SRAM was not designed, we don't comment on the actual area savings or penalty of the 5T SRAM chip as a whole, when compared to the 6T.

### 4.3 Read and Hold Stability

The 5T SRAM provides high RSNM by exploiting the inherent asymmetry of the bitcell. While we have shown that the typical RSNM can be increased, it is more important that sufficient Read and Hold SNM be provided even in the presence of significant local variations. This is especially important in current nanometer technologies, where process and local variations play a critical role in design decisions.

In order to compare the read and hold stability of the 5T bitcells with the reference 6T, Monte Carlo simulations of 1000 iterations each were run at the typical process corner, for a temperature of  $27^{\circ}\text{C}$  with a 1 volt  $V_{DD}$ . Seevinck's least square method [13] was used to determine the RSNM and HSNM. Figure 4.1 shows the Read and Hold SNM distributions for the 6T\_ref, 5T\_unchanged and 5T\_sameArea bitcells described in 4.2.1. We make the following observations. Firstly, the RSNM distribution of 5T\_unchanged is spread wider than 6T\_ref, but is never less than 6T\_ref. Secondly, the three HSNM distributions have almost the same mean, with 5T\_sameArea having a slightly lower value than the other two.

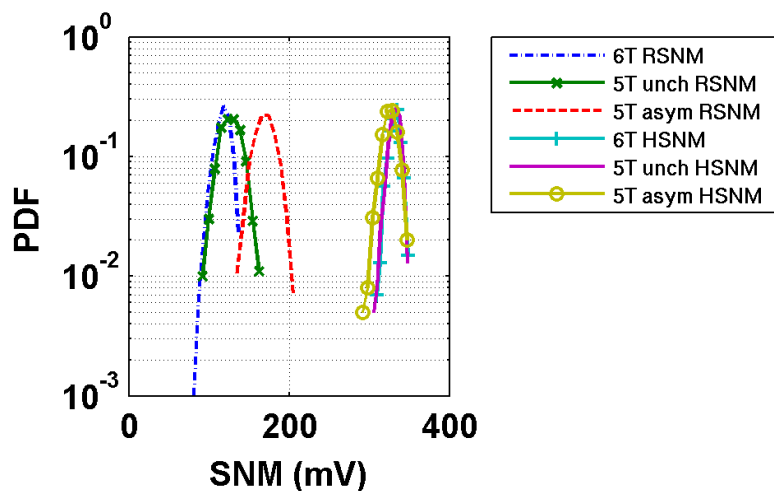


Figure 4.1: Improved statistical read SNM for the asymmetric 5T cell with the same area as the 6T

These observations can be explained as follows. When the access FET is dropped from the 6T, the lower lobe of the butterfly curve in Figure 3.9 is always smaller than the upper lobe. Thus, when the minimum of the two embedded squares is taken, the RSNM of 5T\_unchanged is always larger or the same as the minimum in the 6T case for the same variation. As a result, the spread of the distribution widens towards the right, increasing the mean RSNM. Interestingly, the standard deviation ( $\sigma$ ) of RSNM also increases for the same sized access and drive devices. This is because we are no longer taking the minimum of the upper lobe and lower lobe SNMs since the lower lobe is always smaller. For the 6T case, the distribution of the minimum RSNM has smaller sigma than the distribution of SNM for either lobe. For 5T\_unchanged, the minimum RSNM is the distribution of the lower lobe. So, although its sigma is slightly larger, the higher mean leads to a consistently higher RSNM for the 5T\_unchanged.

As mentioned above, by the definition of RSNM for 6T, it is impossible for the 5T\_unchanged cell to have worse RSNM than 6T\_ref for a given amount of variation. For example, if the RSNM of the two lobes in the 6T are  $RSNM_{6Tu}$  and  $RSNM_{6Tl}$ , and the RSNM of the two lobes of 5T\_unchanged are  $RSNM_{5Tu}$  and  $RSNM_{5Tl}$ , then we have  $RSNM_{5Tu} > RSNM_{5Tl}$ ,  $RSNM_{5Tu} > RSNM_{6Tu}$  and  $RSNM_{5Tl} = RSNM_{6Tl}$ . Now, RSNM is the minimum of the upper and lower lobe RSNMs. Thus for 5T\_unchanged, RSNM is always  $RSNM_{5Tl}$ . If  $RSNM_{6Tu} > RSNM_{6Tl}$ , then RSNM for the 6T is  $RSNM_{6Tl}$ , in which case, the RSNM for the 6T is the same as that for 5T\_unchanged. On the other hand, if  $RSNM_{6Tu} < RSNM_{6Tl}$ , then RSNM for the 6T is  $RSNM_{6Tu}$ . Then, RSNM for 5T\_unchanged is better than that for the 6T, since  $RSNM_{6Tu} < RSNM_{6Tl} = RSNM_{5Tl} = RSNM$  for 5T\_unchanged.

When asymmetry is introduced by widening N1, the mean RSNM for 5T\_sameArea increases significantly when compared to both the 6T and 5T\_unchanged, and the variance of RSNM for 5T\_sameArea reduces when compared to 5T\_unchanged. For the sizes in our example, mean RSNM of the 5T improves by 45% for the same area as the 6T.

Figure 4.2 shows the RSNM of the nominal 5T cell versus the width of the drive transistor N1, keeping the sizes of the other devices constant. Starting with the width that leads to a minimum sized DRC compliant cell (using logic rules), the gain in RSNM is initially almost linear with the

width of N1. Beyond a certain point, gains start to diminish. At this point though, the area penalty would be unacceptable.

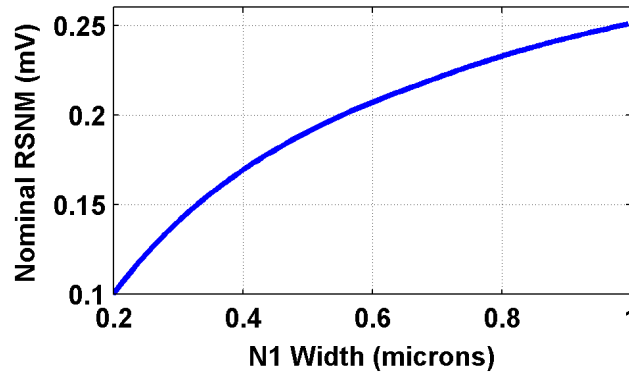


Figure 4.2: 5T RSNM trends with drive transistor width

## 4.4 Read Delay and Drive Current

The drive current of a bitcell is the source-drain current that discharges the bitline during a read. It flows from the terminal of the access NFET that is connected to the BL, through the access NFET and drive NFET, to ground (see section 3.2.2.1). In the case of a 6T bitcell, current either flows from BL to ground or BLB to ground, depending on the data stored in the bitcell. For a 5T bitcell on the other hand, there is no drive current flowing when trying to read a “1” stored in the bitcell. The higher the value of the drive current, the faster the discharge of BL (or BLB) and the lower the read access time.

The current through a transistor is proportional to the W/L ratio of the transistor (Appendix B). Thus, a 5T bitcell that introduces asymmetry by strengthening the drive transistor N1 (e.g. 5T\_sameArea and 5T\_larger described above), helps boost the cell drive current during a read and reduces the Read “0” delay. Without loss of generality, we define the Read “0” delay as the time elapsed between midpoint of the WL rise during WL activation and the BL voltage dropping below

a certain threshold. We arbitrarily choose this to be 900 mV (for  $V_{DD} = 1.0$  V).

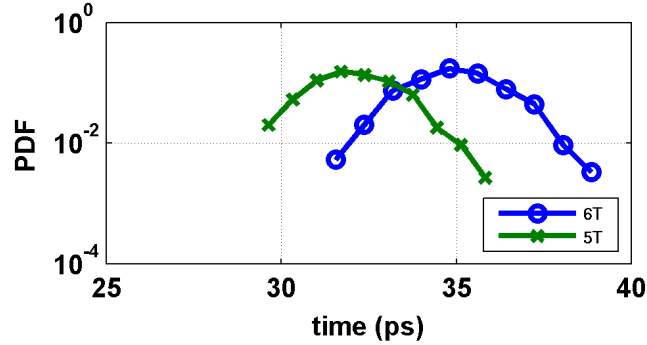


Figure 4.3: For the same bitcell area, mean and sigma of read delay decrease for 5T relative to 6T.

Figure 4.3 compares the Read “0” delay of the asymmetric 5T having a wider drive transistor (5T\_sameArea) with a 6T bitcell (6T\_ref) of the same area. These plots are derived from 1000-iteration MC simulations at the typical process corner, for a temperature of 27°C with a 1 volt  $V_{DD}$ . The 5T bitcell lowers the mean read delay by 8.3% and reduces the standard deviation by 7.7%. This reduced standard deviation means that the asymmetric 5T will have better than an 8.3% improvement in read delay at the  $6\sigma$  point. Note that the Read “0” delay will be improved for any definition of read time since the 5T drive transistor is larger than for the 6T cell of the same total area. In addition, the Total Read “0” delay (defined as the time elapsed between midpoint of the WL rise during WL activation and the midpoint of the sense amplifier output transition) will also be improved for the asymmetric 5T when compared to the 6T, if the same sensing scheme is used (e.g. [11]). This is because the BL discharges faster in the case of the asymmetric 5T due to the higher drive current conducted by the wider drive transistor. The Read “1” delay for this sensing scheme is the same for both since it responds to only BL discharge.

## 4.5 Leakage

Power dissipation is a critical aspect in SRAM design. As technology scales, leakage power dissipation begins to grow in significance. Thus, it is important to evaluate the leakage characteristics of the asymmetric 5T cell and compare it with the conventional 6T bitcell.



There are three sources of leakage in a transistor — subthreshold drain-source leakage, gate tunneling and junction tunneling. The first factor dominates, although the other factors gain significance as technology scales. In this thesis we focus only on subthreshold drain-source leakage. Equation 4.1 gives the sub-threshold leakage current.

$$I_{leak} = I_0 e^{\frac{V_{GS} - V_T}{\eta V_{th}}} (1 - e^{\frac{-V_{DS}}{V_{th}}}) \quad (4.1)$$

where  $I_0 = \mu_0 C_{ox} \frac{W}{L} V_{th}^2 e^{1.8}$ , the thermal voltage  $V_{th} = \frac{kT}{q}$  and

$\mu_0$  = mobility of the carriers at 0 K

$C_{ox}$  = Capacitance per unit area of gate oxide

$W$  = Channel Width

$L$  = Channel Length

$V_{GS}$  = Gate-Source voltage

$V_T$  = Threshold voltage

$\eta$  = Drain Induced Barrier Lowering (DIBL) coefficient

$V_{DS}$  = Drain-Source voltage

$k$  = Boltzmann constant

$T$  = Temperature in Kelvin

$q$  = charge on an electron in Coulombs

There are two aspects of leakage in a memory cell. One is the the bitline leakage through the access FET. As described in section 3.2.2.4, BL leakage affects the read operation and can lead to an incorrect read. The BL leakage is the same for all the 5T cells discussed above as the 6T, since it depends only on the access FET, which is the same for all these bitcells. Note that BL leakage in

the 5T cells occurs only when they are storing a “0” and there is no BL leakage when the cell stores a “1”.

The second aspect of leakage in a memory cell is the leakage through the cross-coupled inverter pair. From equation 4.1, one would expect that the leakage current would increase if the width of the transistor is increased. However, this is not always the case. This is due to a phenomenon called the narrow channel effect, wherein the current first decreases when the width is increased, and then increases again. Figure 4.4 shows this phenomenon.

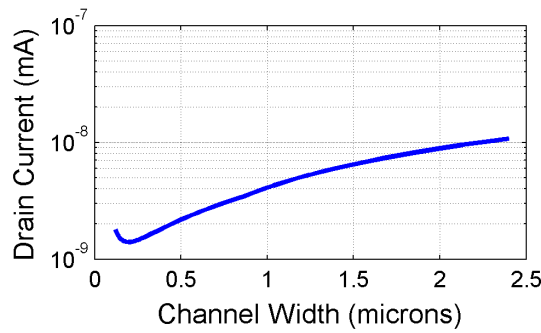


Figure 4.4: Narrow Channel effect on NMOS transistor in 90nm technology

Figure 4.4 plots the drain to source current of an NMOS transistor against the transistor width. According to the transistor current model presented in Appendix B, current should decrease linearly with channel width. However, at very narrow transistor widths, due to a phenomenon called the Narrow Channel Effect ([14]), the current increases instead. We can see from the figure that, at very low widths (e.g.  $0.2\mu\text{m}$  to  $0.5\mu\text{m}$ ), the current hardly changes even if the width is doubled. That is the case for the devices in the bitcells. As a result, the total standby leakage current doesn't vary much compared to the 6T bitcell even when we are increasing device sizes for the 5T bitcells.

To conclude, both bitline leakage and total standby leakage are the same for the 6T and the three 5T bitcells considered. However, if device sizes are much larger than minimum size, then the total standby leakage of a 5T cell would be larger than that of a 6T cell of the same area. However, SRAM bitcells are usually designed to be as small as possible. Thus, it is safe to assume that the 5T

cell would have the same leakage characteristics, both standby and bitline, as a 6T cell of the same area.

## 4.6 RSNM and Read Delay trends with scaling

It is important to see how a particular design technique or circuit scales with technology. The simulations and comparisons presented in the previous subsections were run using a 90 nm design kit. In this section, we will see how the metrics presented earlier scale. We use the Predictive Technology Models (PTMs) [15] for the 45nm, 32nm and 22nm technology nodes.

While the proposed 5T cell provides better RSNM and performance than a 6T cell with the same size in 90nm, it becomes relatively even better in more deeply scaled technologies. Figure 4.5 shows RSNM and read delay distributions obtained with 45nm, 32nm and 22nm PTMs.

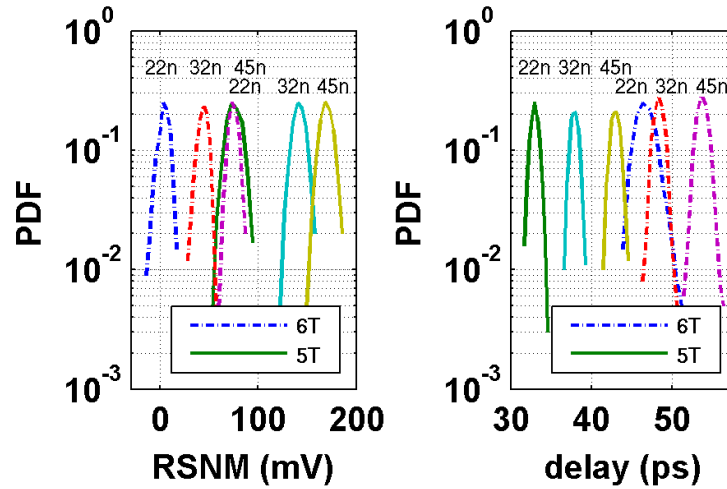


Figure 4.5: Effect of scaling on RSNM and Read delay

The reference 6T bitcells for each of these technologies was chosen so that all dimensions for all the devices were of minimum size. The 5T device dimensions are the same as the reference 6T, except for the drive NMOS transistor, which is made twice as wide. For example, the reference 6T cell in 45nm was chosen to have all widths and lengths as 45nm. It is compared with an asymmetric 5T bitcell whose dimensions are all 45nm, except for N1, which has a width of 90nm. It is not possible to compare the areas of these two bitcells as logic DRC rules are not a part of the PTM

models. However, we can assume that the areas of the two bitcells being compared in each technology are nearly the same, since we are effectively replacing two NMOS transistors of a certain equal width (the drive transistor and the extra access transistor in the 6T) by a single NMOS transistor of double the width (the drive transistor in the 5T).

For each PTM technology, 1000-iteration Monte Carlo simulations for read access time and RSNM were run at the typical process corner, for a temperature of 27°C, with a 1 volt  $V_{DD}$ . The percentage improvement in RSNM and read delay for the 5T cells increase as we move to more advanced technology nodes. For instance, as Figure 4.5 shows, the mean RSNM of the 6T is only around 45 mV for 32nm, but is around 140 mV for the asymmetric 5T — a 3X improvement. Also, the 5T is 30% faster than the 6T in 22nm and exhibits 40% lower delay variation. Finally, the RSNM for the 6T at 22nm has a mean value of 3.5 mV, while that for the 5T has a mean value of 75mV.

Table 4.2 gives the normalized values of various metrics for the three PTM based technologies.

Technology	Bitcell	RSNM( $\mu$ , $\sigma$ )	Read Delay( $\mu$ , $\sigma$ )
45nm	6T	1.0, 1.0	1.0, 1.0
	5T	2.3, 1.3	0.8, 0.75
32nm	6T	1.0, 1.0	1.0, 1.0
	5T	3.3, 1.3	0.78, 0.7
22nm	6T	1.0, 1.0	1.0, 1.0
	5T	22.1, 1.38	0.71, 0.61

Table 4.2: Impact of scaling on metrics (normalized to 6T for each technology)

We can see how the read margin limits scaling of the 6T bitcell to more advance technology nodes, as discussed in the motivation for this thesis. Clearly, the 5T offers an alternative with much better read robustness, speed and variation tolerance when compared to the conventional 6T in future technologies.

# Chapter 5

## Solving the Write Problem

---

### 5.1 The Write Problem

The conflicting requirements for reliable reading and writing of a bitcell pose a challenge. For reliable reading, N1 must be stronger than NA (Figure 5.1). On the other hand, NA needs to be stronger than N1 to ensure reliable writing of a “1”. In a conventional 6T bitcell, this problem is overcome by using a double-ended write strategy. Instead of attempting to write a “1” directly through BL, a “0” is written through BLB. However, this is not possible in a 5T cell due to the absence of a BLB. Thus we need to find a method to reliably write a “1” to the 5T bitcell.

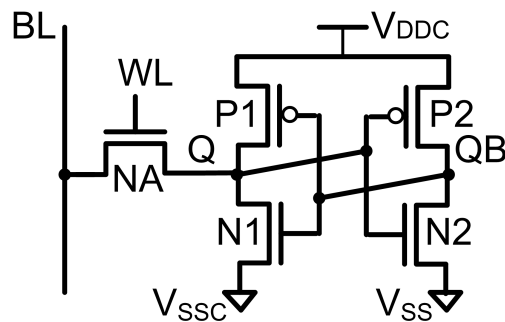


Figure 5.1: 5T bitcell schematic

## 5.2 Write Methodology

Figure 5.2(a) shows the VTCs of the two inverters when writing a “0”. Clearly, there is no problem with writing a “0” as the two VTCs intersect only at one point, meaning the cell has only one stable state, which is the desired state. Also, there is a sufficient write margin (defined as the side of the largest square that can be embedded between the VTCs of the two inverters [16]). However, when attempting to write a “1” through the single access FET, the VTCs of the two inverters intersect at two points (Figure 5.2(b)), which indicates an unsuccessful write. In order to write a “1”, we need to use a mechanism that allows the access transistor to overpower the positive feedback inside the cell. We do this as follows. The BL is precharged to  $V_{DD}$ , and the feedback of the cross-coupled inverters is weakened by either dropping  $V_{DDC}$  (Figure 5.2(c)) or raising  $V_{SSC}$  (Figure 5.2(d)). This technique of weakening the cell feedback has been proposed earlier [17] [18], but has not been applied to a 5T cell. It is similar to the “floating SRC node” technique proposed in [8] in that it attempts to weaken the positive feed-back of the cross-coupled inverters. Now, the curves intersect only once, indicating a successful write “1”. As can be seen from the figures, the write “1” margin is much smaller than the write “0” margin and thus determines the overall WM of the cell.

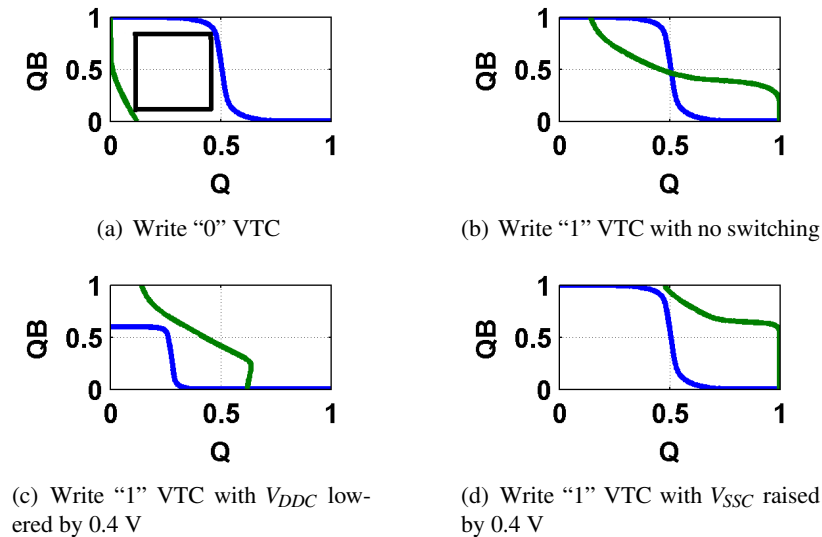


Figure 5.2: Write VTC curves for 5T

Figure 5.3 shows the transient simulation waveforms for a write “1”. The virtual power supply

must be switched back to the normal one before the end of the WL pulse. Otherwise, Q and QB return back to their initial values (0 and 1 respectively), even though they have crossed, and the write is unsuccessful.

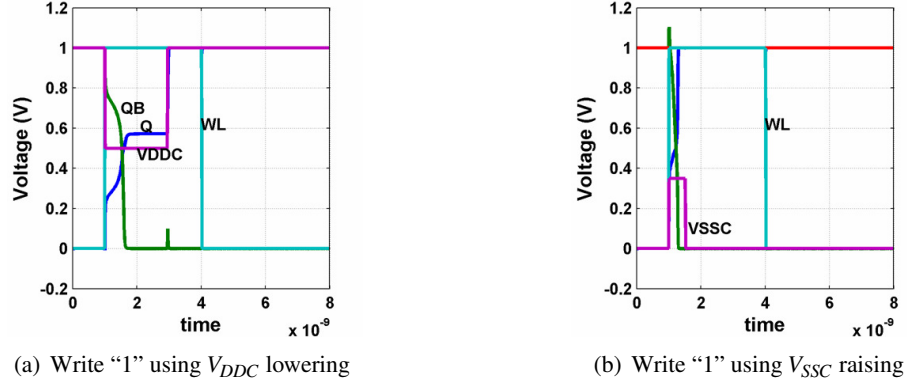


Figure 5.3: Transient simulation for write “1”

### 5.3 Write Margin and Unaccessed Cell Stability

The virtual cell supply (either  $V_{DDC}$  or  $V_{SSC}$ ) can be either generated on-chip, or brought in from off-chip. For ease of testing, the fabricated chip uses off-chip supplies. The virtual cell supply can be shared either row-wise or column-wise. Writing a whole row at a time prevents degradation of hold noise margin for cells in unaccessed columns due to  $V_{DDC}$  lowering or  $V_{SSC}$  raising. On the other hand, sharing the supplies column-wise and writing selected columns of a particular row enables writing and reading of a part of the row, which suits the cache design norm of being able to write or read a part of the cache line according to the offset value. However, this degrades HSNM of cells in the unaccessed rows, risking the loss of their stored values. A similar problem occurs in the 5T cell presented in [8] (see Chapter 2), since the “SRC” node is shared column-wise. Figures 5.4(a) and 5.4(b) show the nominal Hold SNM (HSNM) of an unaccessed cell when  $V_{DDC}$  or  $V_{SSC}$  is lowered or raised respectively. We can see that raising the  $V_{SSC}$  severely impacts the HSNM of unaccessed cells. Lowering the  $V_{DDC}$  has less of an impact. Thus, it is advisable to lower the  $V_{DDC}$  to weaken the feedback when supplies are being shared column-wise.

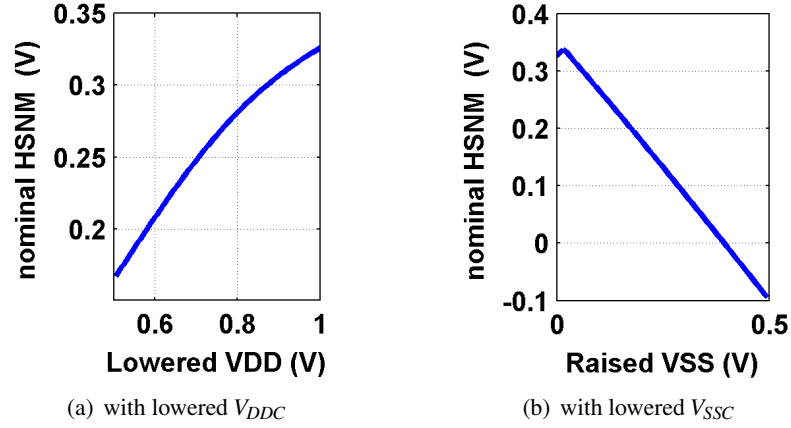


Figure 5.4: Nominal HSNM of unaccessed cells

Figure 5.5 shows the distributions of the HSNM of unaccessed cells and the WM of the accessed cells for different values of the lowered  $V_{DDC}$ , when supplies are shared column-wise.  $V_{DDC}$  needs to be lowered to around 0.2 V to achieve a similar WM as the 6T. However, this leads to an unacceptable HSNM for the unaccessed cells if the virtual rail is routed along the columns. A  $V_{DDC}$  of 0.3-0.4 V provides a reasonable trade-off between the WM and HSNM of unaccessed cells, although it is still much less than the WM of the 6T. Clearly, this is where the conventional 6T scores over the proposed asymmetric 5T. A lower write margin is the price we pay for achieving higher read stability, performance and variation tolerance.

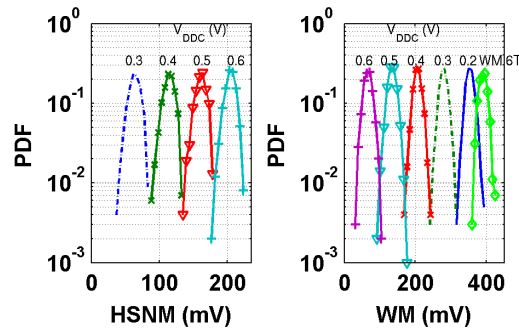


Figure 5.5: Distributions of HSNM of unaccessed cell and WM of accessed cell in a column, when supplies are shared column wise

As Figures 5.2(c) and 5.2(d) show, the WM obtained by lowering  $V_{DDC}$  by a certain amount is more than that obtained by raising  $V_{SSC}$  by the same amount. In addition, the impact of raising



$V_{SSC}$  on the HSNM of unaccessed cells is worse than the impact of lowering  $V_{DDC}$  (Figure 5.3). So, we don't discuss this option further. If the supplies are shared row-wise, there is no constraint on lowering  $V_{DDC}$ . One option for writing individual words along the row is to use a read-writeback approach for the other words, such as the one presented in [6]. In this approach, all the cells in the selected row are first read into temporary registers. Then, the entire row is written by using either  $V_{DDC}$  lowering or  $V_{SSC}$  raising. A mux can be used to select between the new data (for the selected word) or the data in the registers (for the other words), to write into the row. Using this scheme, we ensure that the cells in unaccessed rows are not disturbed, and we also are able to write a part of the row.

## 5.4 Write margin trends with scaling

We have seen in Chapter 4 how the asymmetric 5T bitcell gets better in terms of Read SNM, access time and variability as technology scales. In this section we look at how scaling affects the write margin of the asymmetric 5T.

Figure 5.6 shows the Write Margin distributions obtained with 45nm, 32nm and 22nm PTMs. These simulations use a lowered  $V_{DDC}$  of 0.3 V for the write operation. As in section 4.6, we can assume the cell areas to be approximately the same. We can see that scaling doesn't affect the write margins much, although the write margin of the asymmetric 5T is still significantly lower than that of the conventional 6T.

Technology	Bitcell	Write Margin
45nm	6T	1.0
	5T	0.74
32nm	6T	1.0
	5T	0.76
22nm	6T	1.0
	5T	0.75

Table 5.1: Impact of scaling on Write Margin (normalized to 6T for each technology)

Table 5.1 shows the mean normalized write margin values for 45nm, 32nm and 22nm PTM technologies with respect to the 6T cell in that technology. The write margin of the 5T is roughly

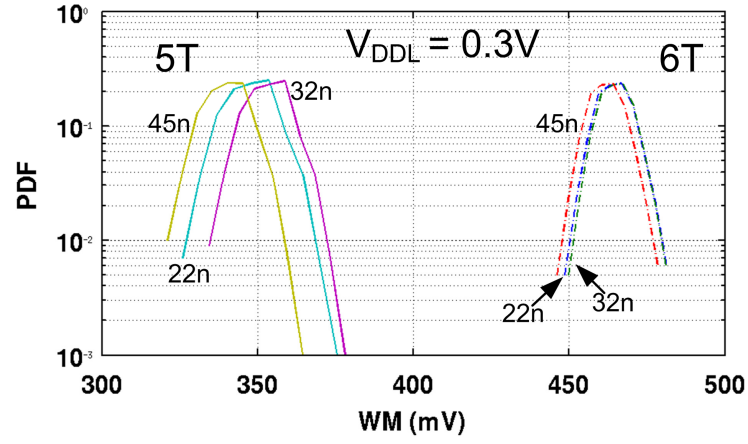


Figure 5.6: Effect of scaling on Write Margin with  $V_{DDL} = 0.3$  V

75% of the 6T across the technologies. Thus, by lowering a  $V_{DDC}$  to a suitable value, a reasonable write margin can still be achieved even at more advanced technologies. In view of the advantages that can be gained by using the asymmetric 5T in future technologies, this makes the asymmetric 5T an attractive alternative to the conventional 6T.

# Chapter 6

## Test Chip Implementation

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### 6.1 Test Chip Architecture

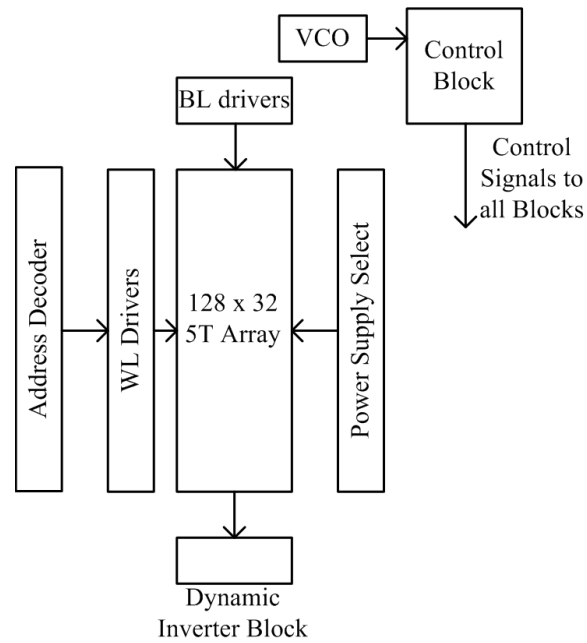


Figure 6.1: Block Diagram of 90nm test chip

A test chip containing a 4 kb SRAM array of 5T bitcells was fabricated in a 90nm bulk CMOS technology. A brief description follows:

- The array has 128 rows, each containing 32 asymmetric 5T bitcells with widened N1 and P2.
- A low  $V_{DD}$  and a high  $V_{SS}$  supply were both brought from off-chip and the write operation was tested with both methods of writing (lowered  $V_{DDC}$  and raised  $V_{SSC}$ ).
- Power supplies were shared row-wise.
- An on-chip VCO provided the option to generate clocks of different frequencies.
- All the control signals such as WL enable, dynamic inverter precharge, alternate  $V_{DDC}/V_{SSC}$  select etc. are generated from the clock signal.
- A full-swing sensing scheme using a dynamic inverter was used to sense the output.
- One dynamic inverter was used per column. In other words, no column multiplexing was used.
- An off-chip control signal selects between the two write methods and a multiplexer is used to select between the normal and alternate  $V_{DD}$  or  $V_{SS}$  during a write.
- A single set of Input/Output Pads for the 32 data bits was used.

Figures 6.1 and 6.2 show the block diagram and the die photograph of the fabricated chip.

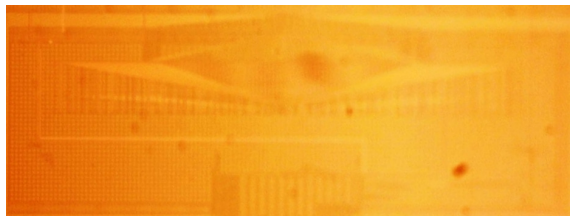


Figure 6.2: Die Photo of 90 nm 5T SRAM

## 6.2 Testing effort and measurements

The chip was tested using a Tektronix<sup>TM</sup> TLA7012 Logic Analyzer and a P6470 Pattern Generator. The following observations were made.

- A “0” could be read correctly only after a two-cycle latency. Moreover, not all locations could successfully read a “0”.
- A “1” could be read correctly only at a few locations. Also, “1” could not be read consistently. That is, if the same location was repeatedly read, “1” was not read correctly after the first read.

It was determined that a timing issue and a design flaw in the read logic were responsible for this behavior. Figure 6.3 shows the Read circuitry.

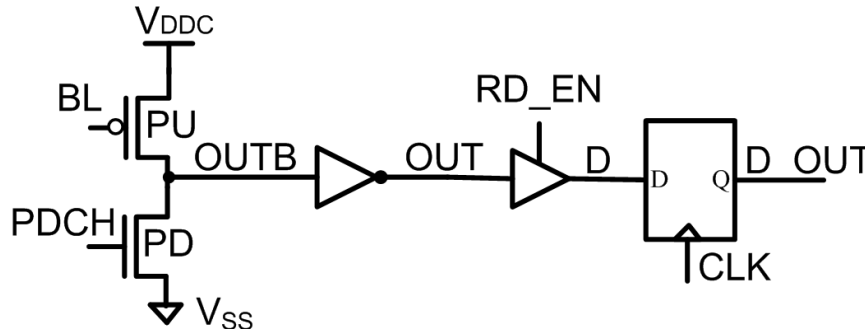


Figure 6.3: Circuit for the Read operation

The control block was designed to generate a pre-discharge(PDCH) pulse in order to discharge the output of the dynamic inverter (OUTB), before the BL is allowed to float. As explained in section 3.2.2.3, if a “1” is being read, PU is off, and OUTB and OUT remain at “0” and “1” respectively. However, this pulse was too short to discharge OUTB. Moreover, there were no knobs

that could be turned to increase the duration of the PDCH pulse. This was confirmed through a simulation in spectre, shown in Figure 6.4. The simulation shown in this figure depicts the read control signals for a repeated read of a particular row. As the figure shows, PDCH does not pulse at the beginning of the read cycle and stays low throughout. As a result, OUTB fails to pre-discharge, due to which a “1” cannot be read correctly. However, if OUTB is initially low when the chip is powered on, we can still read a “1” correctly the first time, which confirms the explanation that the timing generation of the PDCH pulse was faulty. The droop in the BL in this graph is due to BL leakage.

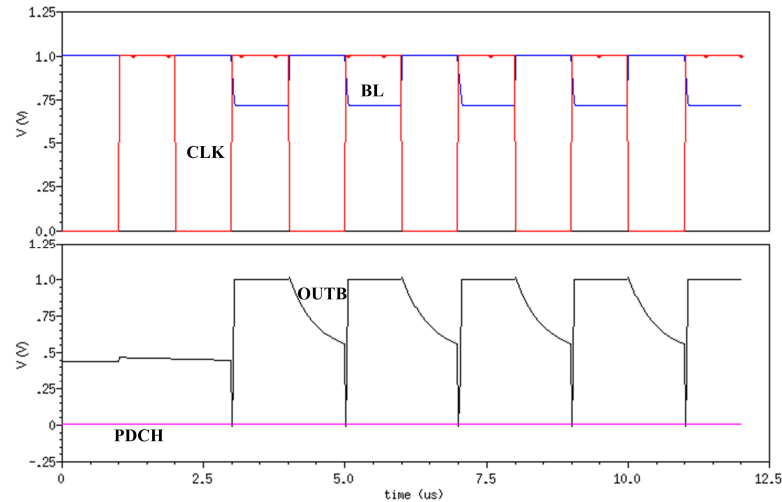


Figure 6.4: Timing diagram for dynamic inverter during read

After the signal on the BL is transferred to the output of the inverter (OUT), it is latched after passing through a tri-state buffer. The second problem is that the RD\_EN signal, the enable signal of the tri-state buffer, doesn't go high sufficiently before the clock edge to satisfy setup time constraints of the flip-flop. The simulation in Figure 6.5 confirms this. We can see that the RD\_EN and CLK signals go high almost at the same time. Again, there are no knobs that can be turned to change the timing of the RD\_EN pulse. As a result, the correct value is read in the next cycle resulting in

a two-cycle lag for the read operation. The first cycle after read is enabled reads garbage data and the second cycle reads correctly.

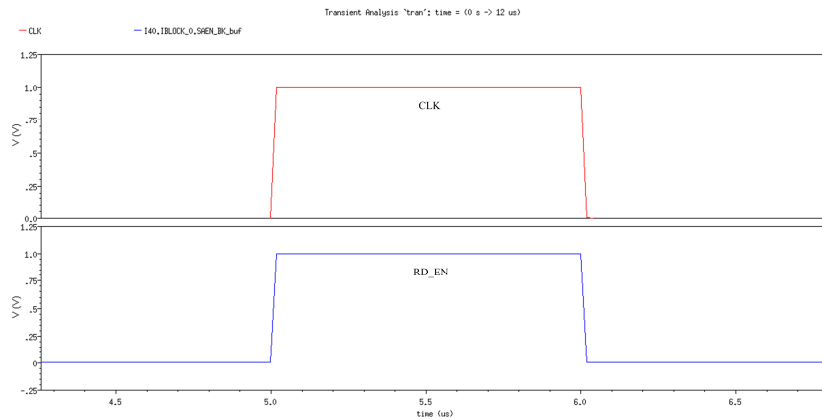


Figure 6.5: Timing diagram for RD\_EN

The two-cycle lag explained above can be seen in Figure 6.6, which shows the Read and Write waveforms for a Write 1 - Read 1 - Write 0 - Read 0 pattern at address 0x22. The signals between the address and data are control signals which determine whether the chip is being read or written, the method that is being used to write, and control signals for the VCO. In this test, the  $V_{DD}$  dropping method is used to write the row.

The problems described above pertain to the peripheral circuits and not the 5T bitcell array. By testing with different data patterns and addresses, some locations were found where we could verify the write and read operations. Row 22 (address 0x22) above was one location where bitline leakage was not significant enough to cause an erroneous read of a “1” as a “0”. In addition, if the output of the dynamic inverter OUTB is low when the chip is powered on, it is possible to read a “1”. In addition, writing and reading the “all 1s” pattern before the “all 0s” pattern ensured that the absence of the PDCH pulse was not a factor. On the other hand, if we attempted to write and read the “all

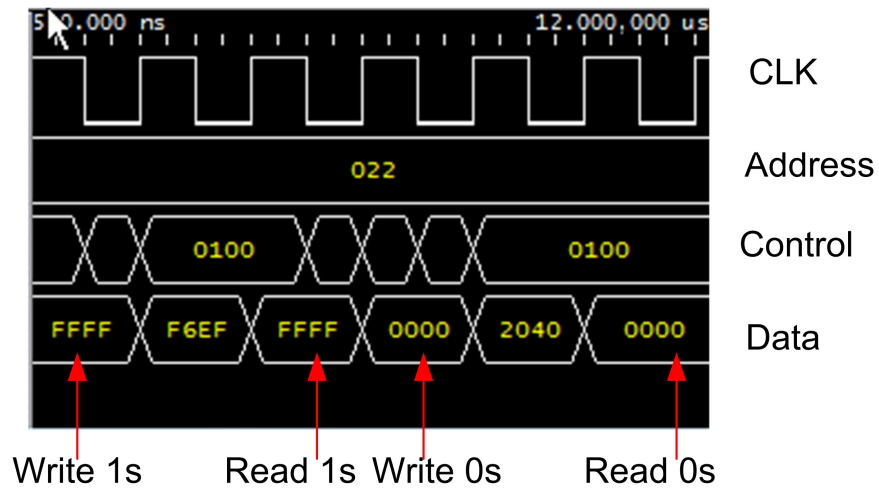


Figure 6.6: Chip Measurement of Read and Write Operations

0s” pattern first, reading the “all 1s” pattern would have certainly failed as this requires the OUTB node to go low, which couldn’t happen due to the problem with the timing of the PDCH pulse.

The problems with the peripheral circuits were addressed in the second version of the 5T SRAM in 45nm. Instead of generating all the control signals from the clock, they were all brought in from off-chip, which gives plenty of flexibility in testing. In addition, the dynamic inverter was replaced with a static inverter, which eliminates the problems that could arise from a faulty timing of the precharge pulse.



# Chapter 7

## Conclusions

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### 7.1 Introduction

This chapter summarizes the project, lists the contributions of this thesis and give future directions for additional research.

### 7.2 Summary

In this thesis, a new 5T SRAM design was presented. The novelty of the design was in using asymmetric sizing to significantly improve the statistical mean of the Read noise margin and read access time when compared to a conventional 6T SRAM, without sacrificing area. The variability in the read access time was also reduced. Lastly, the asymmetric 5T bitcell was found to scale well, offering increasing improvements in RSNM and read access time. The expense to be paid for these gains is a decreased write margin when compared to the conventional 6T and additional overhead for supplying low  $V_{DDC}$  or high  $V_{SSC}$  for the write operation.

Table 7.1 demonstrates the trade-offs that can be made while designing the asymmetric 5T cell. 5T\_sameArea has the same area as the 6T and shows improved metrics. 5T\_unchanged has similar metrics as the 6T, but saves on area. 5T\_larger provides significantly improved metrics at a moderate area penalty. The write margin or writeability progressively decreases as the drive transistor is made wider. This is because a wider drive NFET makes it difficult for the access NFET to win the ratioed

fight with the drive NFET. In other words, raising the storage node voltage to write a “1” to the cell becomes increasingly difficult as the stronger drive transistor keeps sinking the charge. This is reflected in the normalized write margin metrics in the last column of Table 7.1

Metrics Normalized to 6T				
Bitcell	Area	RSNM( $\mu$ , $\sigma$ )	Read Delay( $\mu$ , $\sigma$ )	Write Margin
6T_ref	1.00	1.00, 1.00	1.00, 1.00	1.00
5T_unchanged	0.976	1.08, 1.40	1.00, 1.00	0.78
5T_sameArea	1.00	1.45, 1.36	0.92, 0.92	0.72
5T_larger	1.16	1.98, 1.22	0.88, 0.86	0.65

Table 7.1: 6T vs 5T trade-offs

If the designer is willing to sacrifice some write margin and is more concerned about read stability, access time and variation tolerance, then the 5T SRAM would be a good choice. However, if cell writeability is of foremost importance, then the designer is better off using the conventional 6T bitcell.

### 7.3 Contributions

Note that most of the results in this thesis come from simulation. The fabricated chip was not thoroughly testable due to the reasons explained in Chapter 6. However, it did show that the 5T cell could read and write. Moreover, it did not have a 6T SRAM with which the 5T could be compared. The second chip that was fabricated in 45 nm addresses these issues. The following list points out the contributions of this thesis.

- Introduces the 5T SRAM as an alternative to the conventional 6T SRAM.
- Analyzes the pros and cons of the 5T relative to the 6T.
- Demonstrates the superior statistical read noise margin and access time of the 5T in the presence of local mismatch.
- Suggests a method to reduce variability in read access time.

- Shows how to layout the 5T cell in order to exploit the area gained by removing one access NFET.
- Shows how to use the 5T SRAM to trade-off area with performance and stability.
- Suggests a way to solve the single-ended write problem for the 5T SRAM.
- Analyzes the pros and cons of sharing power supplies row-wise and columnwise.
- Demonstrates the viability of the proposed concept for future technologies.

## 7.4 Future work

The work presented in this thesis can be extended in several ways.

1. Full-swing read operation has been used for both the test chips. Single-ended sensing schemes such as the one suggested by [11] could be applied to the 5T and verified in silicon.
2. As mentioned earlier, this thesis does not include measured results from the 45nm test chip. As of May 2008, the chip has been fabricated and wafer testing environment is being set up. Testing is estimated to commence in July 2008. Results from this chip could confirm the simulation results that the 90nm chip failed to do.
3. Alternative power supplies were brought from off chip for the 90nm 5T SRAM. Methods to generate these voltages on-chip can be explored.
4. While the method of collapsing power supplies to write a “1” works well in the typical case, the low write margin it offers is a drawback. Alternative methods of single-ended write could be explored and applied to the 5T bitcell. In addition, these methods could also be applied to the conventional bitcell and their effectiveness for the two bitcells could be compared.
5. Single-ended operation for the conventional 6T cell could be explored and compared with the asymmetric 5T.

6. Alternative ways to layout the 5T cell could be explored. The array could be laid out in a way that permits exploitation of the extra area to incorporate write assist circuitry to address the write margin problem.

## 6T SRAM

A conventional 6T SRAM consists of a cross-coupled inverter pair and two access NMOS transistors. The access FETS connect the cell to the bitlines. The schematic of the 6T is shown in Figure A.1. The two inverters act as the storage element and store both the data and its complement. The 6T bitcell is symmetrical.

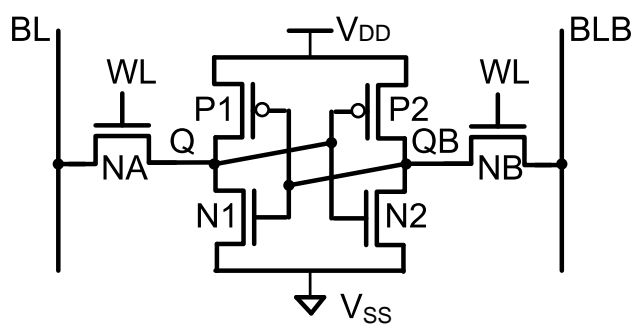


Figure A.1: 6T bitcell schematic

## A.2 Read Operation

Assume that a 0 is stored at Q and both bitlines are precharged to  $V_{DD}$ . The bitlines are allowed to float and the WL is asserted. The values stored in Q and QB are transferred to BL and BLB respectively, through NA and NB. BLB remains at its precharge level and BL starts discharging through NA-N1 (Figure A.2) As a differential voltage develops between BL and BLB, the sense amplifier is activated to speed up the read operation.

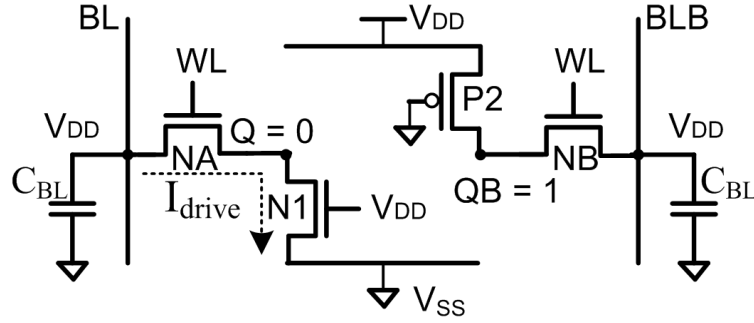


Figure A.2: Simplified model of 6T cell during read ( $Q = 0$ )

When the WL is turned on, the node Q initially rises towards  $V_{DD}$ . The devices in the bitcell need to be carefully sized to avoid Q rising upto  $V_{DD}$  and thus accidentally writing a “1” into the cell. This event is called a read upset. The voltage ripple  $\Delta V$  at Q is given by Equation A.1 ([14])

$$\Delta V = \frac{V_{DSATn} + CR(V_{DD} - V_{Tn}) - \sqrt{V_{DSATn}^2(1 + CR) + CR^2(V_{DD} - V_{Tn})^2}}{CR} \quad (\text{A.1})$$

where CR is the cell ratio, defined as

$$CR = \frac{W_{N1}/L_{N1}}{W_{NA}/L_{NA}} \quad (\text{A.2})$$

To prevent a read upset, the W/L ratio of the drive NFET must be sufficiently larger than that of the access NFET. This ensures that the voltage ripple at the storage node doesn't go above the trip voltage of the other inverter and flip the cell.

### A.3 Write Operation

Assume that a 0 is stored at Q initially. A "1" is written to the cell by driving BL to 1, BLB to 0 and asserting WL. Since the devices have been sized such that the node voltage cannot rise above the trip voltage of the other inverter (to avoid a read upset), it is not possible to actually write a "1" through the access NFET connecting the cell to BL. Instead, we write a "0" to the other node, through BLB. The equivalent circuit is shown in Figure A.3.

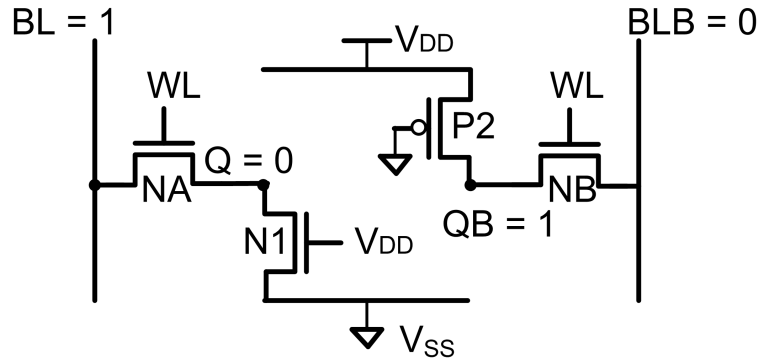


Figure A.3: Simplified model of 6T cell during write ( $Q = 0$ )

In order to reliably write the cell, QB must be pulled below the trip voltage of the inverter P2-N2. The voltage at node QB is given by Equation A.3 ([14]), where  $\mu_p$  and  $\mu_n$  are the mobilities of

holes and electrons respectively.

$$V_{QB} = V_{DD} - V_{Tn} - \sqrt{(V_{DD} - V_{Tn})^2 - 2 \frac{\mu_p}{\mu_n} PR [(V_{DD} - |V_{Tp}|) V_{DSATp} - \frac{V_{DSATp}^2}{2}]} \quad (\text{A.3})$$

where PR is the pull-up ratio, defined as

$$PR = \frac{W_{P2}/L_{P2}}{W_{NB}/L_{NB}} \quad (\text{A.4})$$



## Appendix B

### Current Equations for MOSFET

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This appendix gives an overview of the current equations of an NMOS transistor. Figure B.1 shows the model for manual analysis.

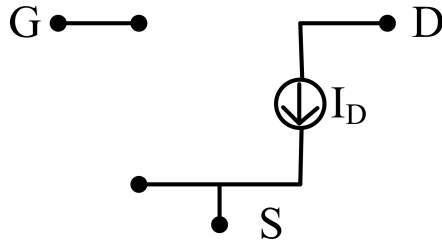


Figure B.1: NMOS current model [14]

There are three modes of operation - linear, saturation and velocity saturation. The current is given by [14]:

$$I_{DS} = k_n' \frac{W}{L} \left[ (V_{GS} - V_T) V_{min} - \frac{V_{min}^2}{2} \right] \quad (\text{B.1})$$

where  $V_{min} = \min(V_{DS}, V_{DSAT}, V_{GS} - V_T)$

with  $V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$  and,

$k_n'$  = process transconductance parameter, which depends on the oxide thickness and permittivity and mobility.

$W =$  Channel width

$L =$  Channel length

$V_{GS} =$  Gate-source voltage

$V_T =$  Threshold voltage

$V_{DS} =$  Drain-source voltage

$V_{DSAT} =$  velocity saturation voltage

$V_{T0} =$  Threshold voltage without body effect

$\gamma =$  Body effect coefficient

$\phi_F =$  Fermi potential

$V_{SB} =$  Source-bulk voltage

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